ABSTRACT OF THE DISCLOSURE

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate having a plurality of spaced apart isolation regions and active regions on the substrate substantially parallel to one another in the column direction. Floating gates are formed in each of the active regions. Control gates are each formed with a substantially vertical face portion by covering a portion of a conductive layer with a protective layer, and performing an anisotropic etch to remove the exposed portion of the conductive layer. An insulation sidewall spacer is formed against the vertical face portion. The control gates have protruding portions that extend over the floating gates.